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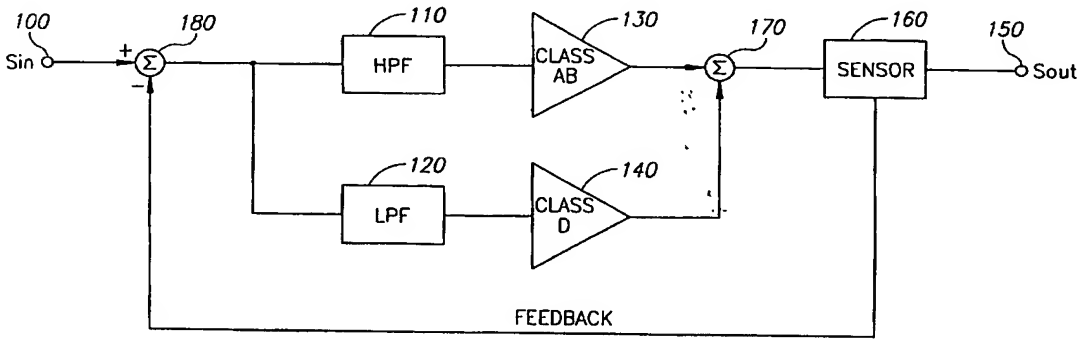
(54) Title: METHOD AND APPARATUS FOR EFFICIENT AMPLIFICATION



(57) Abstract: A circuit is disclosed that utilizes the advantages of a class AB amplifier in the high frequency or low-power range and a class D amplifier in the low frequency or high power range.

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METHOD AND APPARATUS FOR EFFICIENT AMPLIFICATION

FIELD OF THE INVENTION

The invention relates generally to electronic and electric circuits and, more particularly, to efficient amplification of signals.BACKGROUND OF THE INVENTION

Traditionally, power amplifiers are categorized into classes. Class A amplifiers are electrically biased such that the active element of the amplifier (e.g., a transistor) is always in its linear region (i.e., never completely "on" or "off"). While Class A amplifiers provide high fidelity amplification, they dissipate significant power because the active elements of such amplifiers must be biased continually, even when there is no signal input to the amplifier. Thus, the theoretical maximum efficiency in a Class A amplifiers is very low.

Class B amplifiers involve two active elements in a "push-pull" arrangement, whereby one element drives the output while the other element sinks the output. Accordingly, when one element is "on", the other element is "off". This arrangement improves the efficiency of the amplifier; however, when the signal being amplified is small, there may be times when neither of the elements is active, thereby producing crossover distortion.

Class AB amplifiers combine class A and class B circuitry. A small bias is supplied to each of the active elements thereby preventing them from being

completely "off". Thus, Class AB amplifiers feature less crossover distortion than class B amplifiers, and less power dissipation than in Class A amplifiers. By virtue of their reliable performance in amplifying high frequency signals, class AB amplifiers are the solution of choice in most low power or high-frequency applications. Still, the energy consumption of Class AB amplifiers is relatively high, as efficiency levels do not exceed 60 percent. Therefore, class AB amplifiers are generally not suitable for high-power applications.

A class D amplifier, as is known in the art, is a switching amplifier that converts a low-level analog input signal into a high power pulse-width modulated (PWM) output. The switching frequency is much higher (at least ten times) the signal frequency, thereby permitting the high frequency components of the output signal to be removed by a simple filter. In a class D configuration, the load is subjected to a full or half bridge of switches, which permit the load to be pushed or pulled, depending on whether the signal is positive or negative. Insofar as the switches dissipate a minimal amount of power, the Class D amplifier is highly efficient, and may reach efficiency levels of up to 97%. Class D amplifiers have typically been used in low frequency (e.g., 20 kHz) and high power applications (e.g., in the kilo-Watts range), such as heavy motor control and high-power audio. The "noisy" nature of class D amplifiers, however, does not lend itself to high frequency/high fidelity applications, where small distortions may have a significant effect.

There are prior art systems and devices that involve amplification of signals of varying frequency ranges. For example, as is known in the art, certain applications of cathode ray tube (CRT) display devices may operate in either or both of two modes. In "sweep mode", low frequency signals are amplified to control an electron beam of the CRT, accounting for most of the power usage of the control system. In "stroke" mode, high frequency signals are amplified for short periods of time, accounting for a small part of the overall power usage. In "stroke on raster" mode, symbols may be scanned onto the display during the vertical retrace period. This mode combines both high and low frequency symbols. To accommodate the high frequency of the "stroke" mode, such CRT devices must use the highly energy-consuming Class A, B or, typically, AB amplifiers. In both modes, the signal is amplified before being applied to the horizontal or vertical yoke to deflect the electron beam.

SUMMARY OF THE INVENTION

Where an application requires amplification of signals in both low and high frequency ranges, or a wide bandwidth and/or at different power levels, as discussed above, the designer generally must choose between using either a class D or a class AB amplifier, thereby sacrificing either fidelity or efficiency. Embodiments of the present invention include an amplifier that can operate in two different ranges of

frequencies, thereby combining the fidelity of class AB amplifiers for high frequencies with the efficiency of class D amplifiers for low frequencies. According to an embodiment of the present invention, a circuit is provided that combines the advantages of these amplifiers. According to another aspect of the present invention, a power supply is provided that supplies substantially constant voltage irrespective of the current sourced or sinked by the load attached.

BRIEF DESCRIPTION OF THE DRAWINGS

The subject matter regarded as the invention is particularly pointed out and distinctly claimed in the concluding portion of the specification. The invention, however, both as to organization and method of operation, together with objects, features and advantages thereof, may best be understood by reference to the following detailed description when read with the accompanied drawings in which:

Fig. 1 is a block diagram of a circuit for amplifying a signal in accordance with exemplary embodiments of the invention.

Fig. 2 is a schematic diagram of a circuit for amplifying the current of a signal for an inductive load in accordance with some exemplary embodiments of the invention;

Fig. 3 is a schematic diagram of a power supply/power controller circuit for driving a cathode ray tube (CRT) deflection device in accordance with exemplary embodiments of the invention; and

Fig. 4 is a schematic graph illustrating the gain of an amplifier in accordance with exemplary embodiments of the invention as a function of signal frequency.

It will be appreciated that for simplicity and clarity of illustration, elements shown in the figures have not necessarily been drawn accurately or to scale. For example, the dimensions of some of the elements may be exaggerated relative to other elements for clarity or several physical components included in one functional block or element. Further, where considered appropriate, reference numerals may be repeated among the figures to indicate corresponding or analogous elements.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

The invention may be used to drive any type of load; however, the configuration of the particular embodiment may vary depending on the nature of the load. Fig. 1 schematically illustrates an amplifier circuit in accordance with embodiments of the present invention. As shown in Fig. 1, a signal may be input into the amplifier circuit at input terminal 100. A signal with frequency high enough to pass through the high-pass filter 110 is amplified by class AB amplifier 130 and out to

output terminal 150. A signal with frequency low enough to pass through the lowpass filter 120 is amplified by class D amplifier 140 and out to output terminal 150. The high-pass filter 110 and low-pass filter 120 may, for example, be designed such that their gain is identical and/or such that the low cut-off frequency of highpass filter 110 and the high cut-off frequency of lowpass filter 120 are identical; however, this is not necessary if the closed feedback loop is employed. The power signals as amplified by the two amplifiers are mixed at adder 170 and the resulting signal Sout is output to terminal 150. The output signal is sensed, for example, by its voltage or current at sensor 160, and fed back to adder 180.

Using the feedback loop as shown, the amplification is properly distributed between the branches such that each branch operates as necessary depending on the signal frequency. In this way, the entire circuit may operate with a uniform gain for a continuous range of frequencies. Variations of the basic circuit design of Fig. 1 may be used to amplify a signal supplied to various type of loads, for example, inductive, capacitive and resistive loads. For such loads, the embodiment may be modified to compensate for phase shift distortion, as described below. It will be appreciated by those of ordinary skill in the art that the high-pass filter 120 and low-pass filter 130 may be comprised of multiple components (e.g., resistors, inductors, capacitors, etc.), or may be comprised of commercially available filters, depending on the desired results. It will further be appreciated that the elements comprising the high-pass filter 110 and low-pass filter 120 may be placed anywhere

in the circuit and not necessarily in the relation to the class AB amplifier 130 and class D amplifier 140 as shown in Fig. 1.

Circuits according to embodiments of the present invention may be used to drive an inductive load, such as a deflection coil (yoke) of a cathode ray tube (CRT). As is known in the art, a CRT may have a "stroke on raster" mode, which combines both low and high frequency signals. The present invention is therefore particularly suitable for amplifying deflection signals to a yoke in a CRT in that the signal to be amplified may be of high or low frequency. However, it will be apparent to persons skilled in the art that the invention may also be suitable for any other system or device in which signals of varying frequency ranges, or a wide range of frequencies, are amplified to provide more power efficient amplification.

Due to the pulse-width modulation (PWM) output of Class D amplifiers, they are generally considered too "noisy" for use in amplifying CRT deflection signals because even small distortions in amplification in a CRT can cause significant screen "jitter." According to principles of the present invention, the efficiency of class D amplifiers can be used in a CRT by amplifying only signals of sufficiently low frequencies, for which the PWM noise is insignificant. In contrast, for the high frequency signals, a class AB amplifier circuit is used. Thus, the present invention integrates two amplification functions into one device and, therefore, the invention

may also reduce the size and cost of circuitry associated with the device using the invention.

Although the invention is described herein in the context of a dual-mode CRT device, it should be appreciated that the invention may be used in conjunction with any other type of device, system, circuit, etc., where amplification of signals at varying frequencies or wide bandwidth may be needed. Moreover, the principles of the invention may be used to amplify signals having different ranges of power.

In a CRT stroke on raster scan, the frequencies of both the horizontal and/or vertical deflection signals may vary dramatically, depending on the mode of operation. Thus, an embodiment of the present invention may use a class D amplifier to amplify deflection signals at both low frequencies, e.g., for "sweep" mode deflection signals at frequencies on the order of approximately 15 kHz and 50-60 Hz, and a class AB amplifier to amplify high frequencies, e.g., for "stroke" mode deflection signals at frequencies on the order of approximately 100-2000 kHz.

Fig. 2 schematically illustrates an amplification circuit in accordance with embodiments of the invention. Thus, for example, a circuit similar to that shown in Fig. 2 may be used for each of the horizontal and vertical deflection signal amplification circuits of a CRT. The characteristics of the elements chosen may vary depending on the different expected frequencies of the deflection input signal and on the desired power gain. Moreover, some circuit components may be added or

omitted as necessary for a particular application. It should be appreciated that the applicability of the circuit of Fig. 2 is not limited to CRT applications, and similar circuits may be used in conjunction with any other application where signal amplification based on frequency discrimination may be advantageous. Other applications where such a circuit may be useful include but are not limited to wide bandwidth magnetic deflection devices, wide bandwidth scanning machines, wide bandwidth power supplies, wide bandwidth motors, valve and actuator controls, wide bandwidth reactive load drivers, high speed active magnetic bearings, high speed MRIs, wide bandwidth vibration cancellation machines, wide bandwidth power transducers, high power high efficiency low distortion audio amplifiers, high efficiency sonar transducer drivers, high efficiency high sped/power LED-diode excitation circuits, high efficiency noise cancellation circuits, etc. The diagrams and explanations of the embodiments described herein are not intended as limitations on the scope of the invention.

The circuit according to the embodiment of Fig. 2 receives an input signal at terminal 302 and produces a uniformly amplified, high-fidelity output signal at the CRT yoke or deflection coil 336. As explained below, by virtue of the current feedback arrangement shown, a signal of low frequency or DC is amplified predominantly through the class D amplifier 318, whereas a signal of high frequency is amplified predominantly through the class AB amplifier 312. In addition, the circuit

as shown ensures that the gain at the CRT is substantially constant regardless of whether one amplifier or the other, or both, is in operation.

To accomplish these and other goals, the circuit may be equipped with an error amplifier 306. The error amplifier 306 receives an input responsive to the sum of the current passing through resistor 304 and the current passing through resistor 332 and capacitor 352 (representing the output signal to the CRT 336, which is 180° out of phase with the input signal). In order to improve the efficiency of the circuit, the resistance of resistor 334 may be decreased and an operational amplifier 350 may be added. The sum of these currents, representing the error of the amplification (using the sum of the class D and class AB amplifiers) is amplified by error amplifier 306.

The signal output from error amplifier 306 is diverted to the class D or class AB amplifier subcircuit, or a combination of both, based on its frequency. Thus, if the deflection signal is of a sufficiently high frequency, e.g., greater than frequency f1, the signal will be amplified by a class AB amplifier 312. Resistor 310 and a capacitor 308 are arranged in a high-pass arrangement according to principles known in the art. Frequency f1 is the frequency for which the current output from the class AB branch is equal to the output of the class D branch. At frequencies greater or less than f1, the two branches operate together in a ratio of current outputs determined by the signal frequency. The components that determine frequency f1 include 310, 348,

314, 316, 320, 326 and 308. High impedance elements 348 and 326 are added to the branches in order to add the currents from the two branches together. Capacitor 362 may be added in parallel to inductor 326 as a trap for the modulating frequency of the class D amplifier, thus reducing output noise of the amplifier. Components 324 and 338 may be used to stabilize the class D branch at higher frequencies.

In an exemplary embodiment of the present invention, the components may have the following values: capacitor 338 may be for example 100 nF; resistor 324 may be 5Ω; resistor 310 may be 10kΩ; resistor 348 may be 5Ω; capacitor 314 may be 1 μF; resistor 316 may be 12kΩ; capacitor 320 may be 100pF; inductor 326 may be 10μH; capacitor 308 may be 10nF; inductor 344 may be 1.5 μH; capacitor 346 may be 80nF; resistor 328 may be 175 Ω; capacitor 330 may be 0.1 μF (assuming for example, a 20μH yoke); resistor 342 may be 10kΩ; capacitor 340 may be 0.1 μF; capacitor 360 may be 150 nF; capacitor 352 may be 30 pF; resistor 334 may be 0.1 Ω; capacitor 362 may be 1.5 nF; and resistor 332 may be 1 kΩ. While the characteristic values of most of the components listed above may be varied by approximately an order of magnitude, the value of two components should be specified more precisely, namely, resistor 334, resistor 332 and resistor 304.

Thus, in the above configuration, any high frequency input signal is amplified predominantly by the class AB amplifier 312, and any low frequency input signal is amplified predominantly by class D amplifier 318. After amplification by either class

amplifier, the amplified signal is received at the CRT deflection coil 336, and sent to ground via resistor 334. This current is sampled as part of the feedback loop to the error amplifier 306. If an operational amplifier 350 is used, its gain multiplied by the resistance of resistor 334 represents a new, typically higher, effective resistance

It should be noted that when the load being driven, e.g., the CRT deflection coil 336, is inductive, its increased impedance at higher frequencies introduces phase shift distortion. This phase-shift error should be corrected at those high frequencies. This may be done, as shown in the embodiment of Fig. 2, by resistor 328 and capacitor 330, as well as by capacitor 340 and resistor 342. These elements, in combination, function to correct the phase shift distortion that may be introduced at higher frequencies. Due to the high impedance of the capacitors at low frequencies and DC voltages, the phase-shift correction components do not affect performance at low frequencies. The function of optional switch 364, capacitor 366 and resistor 368 is discussed below with regard to shifting the cut-off frequency of the amplifier.

The combination of resistor 324 and capacitor 338 provide low impedance at high frequencies, thereby diverting current from inductor 326, stabilizing the class D subcircuit 358 at such high frequencies, and limiting the contribution of class D sub-circuit 358 to the current at the deflection coil 336. Likewise, resistor 348 and capacitor 314 provide high impedance at low frequencies, thereby decreasing current

from class AB subcircuit 356, stabilizing the class AB subcircuit 356 at low frequencies, and limiting the contribution of class AB sub-circuit 356 to the current at the deflection coil 336.

The horizontal deflection signal requires retrace of the electron beam at a high rate (i.e., high retrace ratio) and a high current that is typically beyond the capabilities of the overall amplifier configuration due to present technological limitations. Therefore, in an amplifier circuit used to amplify the horizontal deflection signal, switches 352 and 354 may be inserted to prevent the amplifiers from such overload. During normal operation, switches 352 and 354 are closed; however, during rapid retrace, the switches are open and capacitor 360 is charged, creating a half-sine wave at a frequency determined by the characteristics of capacitor 360 and deflection coil 336. Switch 354 helps minimize power loss during retrace. The action is similar to a pendulum, in which the power stored in the deflection coil at the end of a line scanned serves to return the electron beam approximately back to the starting point. This technique is known and used in nearly all televisions produced today.

Parasitic capacitances around error amplifier 306 cause a reduction in the drop-off frequency of the overall circuit, f2 and increase instability in the circuit. Therefore, capacitor 352 may serve to compensate and restrain this tendency to instability created by the parasitic capacitances.

Inductor coil 344 and capacitor 346 operate as a lowpass filter to eliminate the modulation frequency of the class D amplifier. Those of ordinary skill in the art will appreciate that the components should be chosen so as not to narrow the bandwidth of the amplifier. As these components transmit great amounts of power in short periods of time, they should preferably be high quality components, such as NPO/COG capacitors.

In an embodiment of the present invention, the current passing through resistor 334 represents the sum of currents put out by both the amplifier branches, which is fed back to error amplifier 306 serving the entire circuit operating as a whole. The result of the feedback loop taking its input from the two amplifier branches is a unified closed circuit that operates as one amplifier with an overall gain.

The class D amplifier may operate in a full bridge or half bridge configuration. In a full bridge configuration, one power supply suffices to provide the amplifier with power; however, the power required to activate the switching elements in this configuration tends to decrease the overall efficiency of the amplifier due to the use of two pairs of switching elements. In a half bridge configuration, it is convenient to have both positive and negative power supplies connected to the amplifier. In a full bridge configuration, however, the power required to activate the switching elements tends to decrease the overall efficiency of the amplifier.

In order to utilize the class D amplifier in the manner described above, any power supply adequate for the class D amplifier may be used. One power supply/power controller circuit that may be used to supply a steady voltage relatively irrespective of the current being sourced or sunk is described in Fig. 3. One purpose of the power supply described in Fig. 3 is to convert a floating voltage (Vcc) into positive and negative voltages relative to a ground. Preferably, each of these voltage sources, i.e., positive and negative, should be able to supply current and receive excess current without varying its voltage. In addition, preferably, excess current to one voltage supply does not become wasted, e.g., become dissipated as heat, but rather is passed through to charge the other voltage supply, thereby optimizing efficiency.

In Fig. 3, the voltage divider comprised of resistors 408 and 410 divides the floating DC voltage Vcc at terminals 400. The PWM controller 402 may operate to open and close switches 404 and 406, such that the two are never closed simultaneously. By connecting the end of inductor 412 opposite to the PWM controller to ground, and tapping the voltage opposite capacitors 414 and 416, stable voltages relatively irrespective of current sourced or sinked may be obtained at terminals 418 and 420. Specifically, if the current across capacitor 416 becomes greater than the current across capacitor 414, capacitor 416 discharges while the voltage potential between terminals 418 and 420 remains constant Vcc. Thus, as the voltage across 414 tends to increase, the voltage divider comprising resistors 408

and 410 alters the duty cycle of the PWM controller such that switch 404 is closed for longer durations, thereby compensating for the imbalance. As capacitor 414 discharges, inductor 412 is charged. When switch 406 is closed, the charged inductor discharges across capacitor 416. Thus, the charge stored across capacitor 414 is transferred to capacitor 416 using inductor 412 and switches 404 and 406. The theoretical basis for the efficiency is that the energy across one capacitor, i.e., $CV^2/2$, is transferred to the inductor, i.e., $LI^2/2$, and then to the other capacitor. Thus, the difference between the voltages at terminals 418 and 420 is Vcc. The duty cycle established by the PWM controller determines the values of Vpos at terminal 418 and Vneg at terminal 420. The embodiment of the power supply described provides a substantially constant voltage for power within an operating range.

In an exemplary embodiment of the present invention, PWM controller 402 may be a commercially available controller for a class D amplifier; inductor 412 may be 10μH; capacitors 414 and 416 may be 100 μF; resistors 408 and 410 may be 10kΩ.

In the embodiment shown in Fig. 2, a half bridge was chosen due to considerations of efficiency and simplicity. Thus, positive and negative power supplies are provided that need to work in both source and sink mode. It will be appreciated by those of skill in the art that alternatively, a full bridge or other configuration may be employed with similar effect in accordance with the present

invention. Alternately, those of skill in the art will recognize that a full bridge may be used, accompanied by appropriate alterations in the circuitry.

It will be appreciated by those of skill in the art that a circuit for amplification of both horizontal and vertical deflection signals may be constructed by combining two circuits such as shown in Fig. 2, one for each input signal (Xin and Yin) and each having a separate output signal across the appropriate yoke or deflection coil (Xout across the horizontal deflection coil and Yout across the vertical deflection coil). In such a configuration, both class D amplifiers may be controlled by a single power supply/power controller as shown in Fig. 3.

The resultant overall gain of the amplifier of Fig. 2 is illustrated schematically in Fig. 4. The amplification of the subcircuit containing the class D amplifier is shown by curve 500, where f1 is the frequency at which the amplification by the class D subcircuit is halved. The amplification of the subcircuit containing the class AB amplifier is shown by curve 502, where f1 and f2 are frequencies at which the amplification by the class AB subcircuit is halved. Thus, a signal having frequency up to f1 is amplified predominantly by the class D sub-circuit, whereas a signal having frequency between f_1 and f_2 is amplified predominantly by the class AB sub-circuit. The sum of the amplification of the two sub-circuits is shown by curve 504. It will be appreciated that the arrangement shown in the above embodiments result in substantially constant gain regardless of whether amplification is performed by the class AB or class D subcircuits, or both. Moreover, at and around frequency

f_1, the overall gain of the entire circuit is a constant Ao even though both sub-circuits are in operation.

In some embodiments of the present invention, it may be desirable to shift the cut-off frequency for certain applications, for example, in order to narrow the bandwidth of the amplifier. In such embodiments of the present invention, therefore, the cut-off frequency may be shifted, for example, from f2 to lower frequency f2', as shown in Fig. 4, thereby narrowing the bandwidth of the amplifier. This may optionally be accomplished, for example, as shown in Fig. 2, by placing an impedance, such as resistor 368 and capacitor 366, in parallel with capacitor 340 and resistor 342. In an exemplary embodiment of the invention, this additional impedance may be selectively connectable, for example, by switch 364, which may control shifting cut-off frequency f2 to f2'. In an embodiment of the invention, the additional impedance may optionally be altered to variably adjust the cut-off frequency.

While the invention has been described with respect to a limited number of embodiments, it will be appreciated that many variations, modifications and other applications of the invention may be made.

Embodiments of the present invention may include other apparatuses for performing the operations herein. Such apparatuses may integrate the elements of the amplifiers discussed, or may comprise alternative components to carry out the

same purpose. It will be appreciated by persons skilled in the art that the present invention is not limited to what has been particularly shown and described hereinabove. Rather the scope of the present invention is defined only by the claims, which follow:

CLAIMS

What is claimed is:

1. A circuit for receiving an input signal and providing an output signal comprising:

a first circuit branch including a first amplifying element for amplifying the input signal when the frequency is below a pre-determined frequency; and

a second circuit branch connected in parallel with said first circuit branch and including a second amplifying element for amplifying the input signal when the frequency is above a pre-determined frequency.

2. A circuit as in Claim 1 wherein the first amplifying element comprises a Class D amplifier.

3. A circuit as in Claim 1 wherein the second amplifying element comprises an amplifier selected from the group consisting of Class A, Class B and Class AB amplifier.

4. A circuit as in Claim 2 wherein the second amplifying element comprises an amplifier selected from the group consisting of Class A, Class B and Class AB amplifier.

5. A circuit as in Claim 3 further comprising a power controller connected to the Class D amplifier to control the power supplied to the Class D amplifier.

6. A circuit as in Claim 1, wherein the second circuit branch includes a high pass filter.

7. A circuit as in Claim 7, wherein the high pass filter comprises a capacitor.

8. A circuit as in Claim 1 wherein the first branch comprises a low pass filter.

9. A circuit as in Claim 9, wherein the low pass filter comprises an inductor.

10. A circuit as in Claim 7, wherein the first branch comprises a low pass filter.

11. A circuit as in Claim 11, wherein the low pass filter comprises an inductor.

12. A circuit as in Claim 1, wherein a feedback signal corresponding to the sum of a signal produced by the first circuit branch and a signal produced by the second circuit branch is mixed with the input signal.

13. A circuit as in Claim 4 wherein the input signal comprises a horizontal deflection signal for a cathode ray tube.

14. A circuit as in Claim 4 wherein the input signal comprises a vertical deflection signal for a cathode ray tube.

15. A circuit as claimed in claim 1, wherein said second amplifying element of said second circuit branch has a cut-off frequency, and wherein said cut-off frequency may be adjusted.

16. A circuit as claimed in claim 1, wherein said cut-off frequency may be variably adjusted.

17. A method of amplifying an electric signal comprising:

amplifying the electric signal predominantly using a first amplifying element when the frequency of the signal is below a pre-determined frequency; and

amplifying the electric signal predominantly using a second amplifying element when the frequency of the signal is above the pre-determined frequency.

18. The method of Claim 17 wherein the first amplifying element comprises a Class D amplifier.

19. The method of Claim 17 wherein the second amplifying element includes an amplifier selected from the group consisting of Class A, Class B and Class AB amplifier.

20. The method of Claim 18 wherein the second amplifying element includes an amplifier selected from the group consisting of Class A, Class B and Class AB amplifier.

21. The method of Claim 20 wherein the electric signal includes a horizontal deflection signal in a cathode ray tube.

22. The method of Claim 20 wherein the electric signal includes a vertical deflection signal in a cathode ray tube.

23. The method of claim 17, further comprising:

adding to the electric signal a second electric signal corresponding to the sum of the signals produced by the first and second amplifying elements.

24. A circuit for receiving an input signal and providing an output signal comprising:

a first circuit branch including a first amplifying element; and

a second circuit branch connected in parallel with said first circuit branch and including a second amplifying element,

wherein said input signal passes predominantly through said first amplifying element if the frequency of the input signal is below a pre-determined frequency and wherein said input signal passes predominantly through said second amplifying element if the frequency of the input signal is above said pre-determined frequency.

25. Apparatus for supplying substantially constant voltage substantially irrespective of the current sourced or sinked within an operating range of power to a load comprising:

a voltage source to provide a voltage between first and second terminals;

a pulse width modulation controller connected to receive at least a portion of the voltage between the first and second terminals of said voltage source and to produce an output;

an inductor having a first terminal connected to the output of the pulse width modulation controller and a second terminal connected to ground;

a first capacitor connected between the first terminal of the voltage source and ground; and

a second capacitor connected between the second terminal of the voltage source and ground,

wherein the voltage between the first terminal of the voltage source and ground is substantially constant.

26. Apparatus in claim 25, wherein the voltage between the first terminal of the voltage source and ground is adapted to supply power to a class D amplifier.

27. Apparatus in claim 26, wherein the voltage between the second terminal of the voltage source and ground is adapted to supply power to a class D amplifier.

28. A circuit as in claim 7, wherein the power controller comprises:

a voltage source to provide a voltage between first and second terminals;

a pulse width modulation controller connected to receive at least a portion of the voltage between said first and second terminals of said voltage source and to produce an output;

an inductor having a first terminal connected to the output of the pulse width modulation controller and a second terminal connected to ground;

a first capacitor connected between the first terminal of the voltage source and ground; and

a second capacitor connected between the second terminal of the voltage source and ground, wherein the class D amplifier is supplied with voltage between the first terminal of the voltage source and ground.

29. A circuit as in claim 28, wherein the class D amplifier is supplied with voltage between the second terminal of the voltage source and ground.

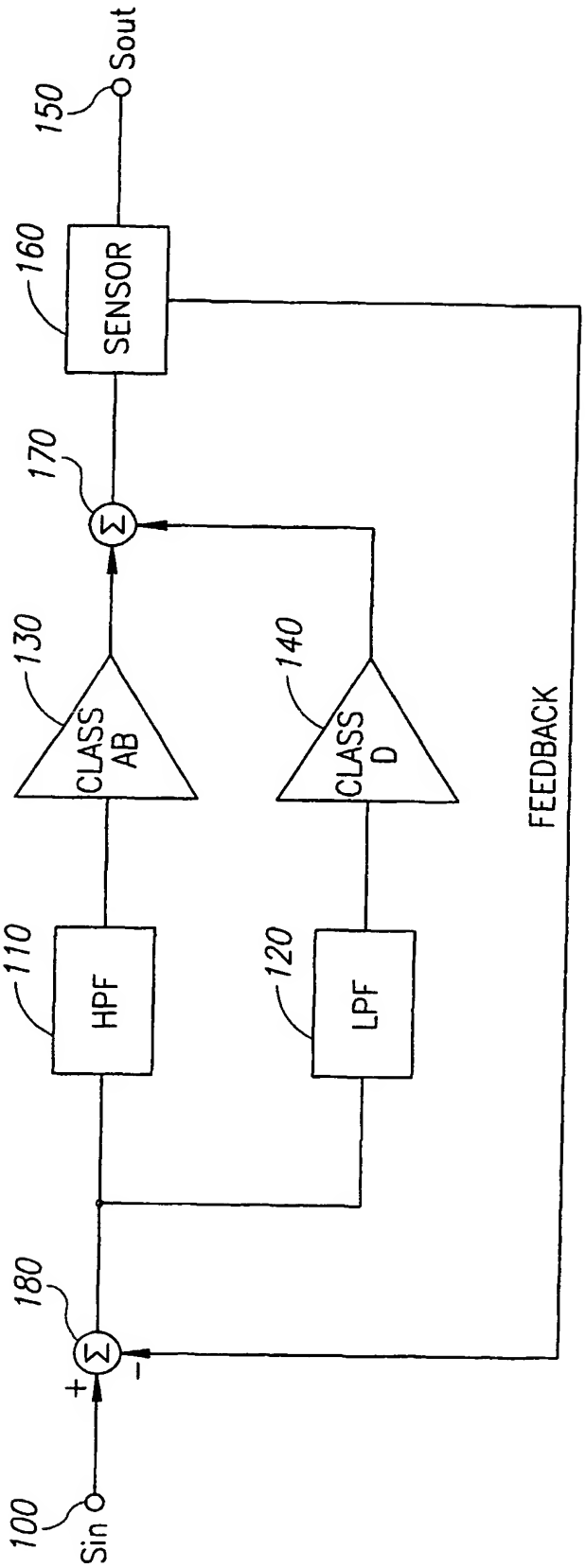
Sout
150
160
SENSOR
170
130
CLASS AB
140
CLASS D
FEEDBACK
110
HPF
120
LPF
180
+
-
100
Sin

FIG.1

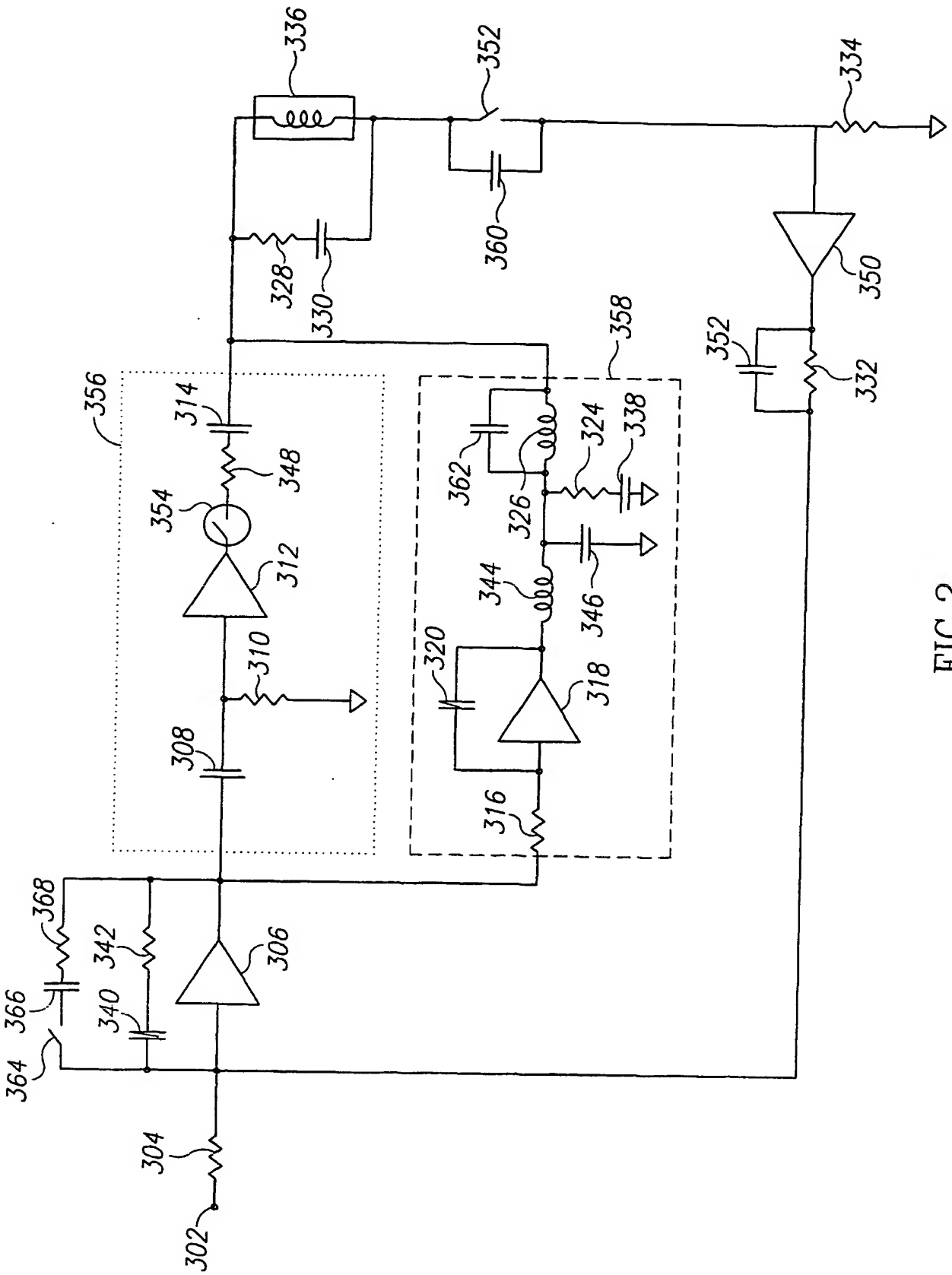
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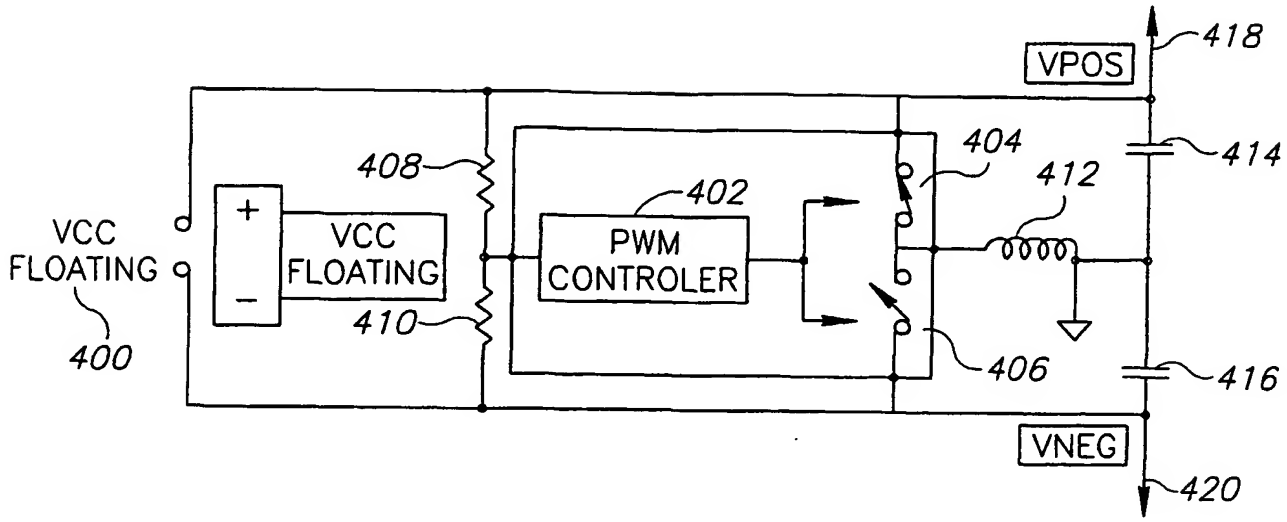
FIG.2


VPOS
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414
404
412
408
402
VCC
FLOATING
VCC
FLOATING
PWM
CONTROLER
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406
416
400
VNEG
420

FIG.3

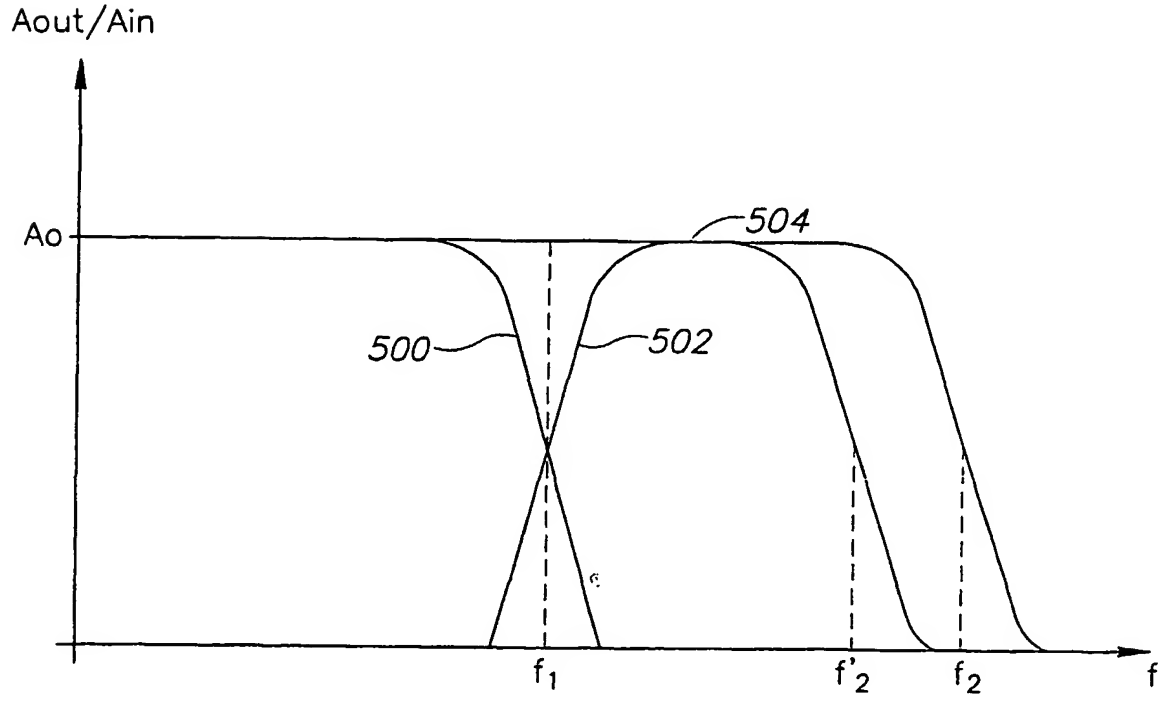
Aout/Ain
Ao
504
500
502
f1
f'2
f2
f

FIG.4

INTERNATIONAL SEARCH REPORT

International Application No
PCT/IL 03/01059

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03F1/02 H02M3/158 H03F3/21

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03F H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 4 346 349 A (YOKOYAMA KENJI) 24 August 1982 (1982-08-24) the whole document	1-4, 6-12, 15-20, 23,24 5,13,14, 21,22, 25-29
X Y	US 3 733 514 A (GARUTS V) 15 May 1973 (1973-05-15) abstract	1,17,24 13,14, 21,22
Y	WO 02/15387 A (CAMP WILLIAM O JR ; DENT PAUL W (US); ERICSSON INC (US)) 21 February 2002 (2002-02-21) page 44, paragraph 3; figure 21C	5,25-29

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents :

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"O" document referring to an oral disclosure, use, exhibition or other means

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Date of the actual completion of the international search	Date of mailing of the international search report
11 March 2004	18/03/2004

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Van den Doel, J

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/IL 03/01059

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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